ABSTRACT
A third-order sigma-delta (Σ - Δ) modulator implementation in a Digital Power Amplifier is presented in this paper. The operation is obtained by using a novel combination of architectural features, proper circuit structure selections, specific clocking strategies, and efficient circuit optimization algorithms. Measurement results from fabricated CMOS chip prototypes show a good match with simulations.

1. INTRODUCTION
Sigma-delta (Σ - Δ) modulators have been widely used over the last few decades, in various signal processing applications. Usually, for improved signal-to-noise performances, higher order modulators are utilized in these applications including the conventional A/D and D/A converters as well as the use in the design of the Finite Impulse Response (FIR) and the Infinite Impulse Response (IIR) filters, AM/FM modulators, multipliers and synchronizers and so on[1][2]. A major reason for the popularity of Σ - Δ architectures lies in their ability to trade bandwidth with quantization noise. These circuits lead to a reduction in expensive hardware and help in speeding up computations as well provide higher resolution in comparison to traditional analogue circuitry. Furthermore, as the Σ - Δ modulated signals are usually restricted to take values of {-1, 0, +1}, the Σ - Δ based signal processing architecture provides programmability and flexibility in the circuits. The 1-bit output of these modulators removes the need for multi-bit multipliers and hence decreases the complexity and cost of the circuit. The resolution is also improved due to over-sampling before modulation. Multipliers can be entirely eliminated from the circuit by using shift registers to process the 1-bit output of the modulator [3]. Though multipliers have become cheaper over the last decade, multi-bit multipliers are still expensive for VLSI implementations. At another side, the designed architecture can meet higher bit resolution at lower cost, which makes it very lucrative. All these features make Σ - Δ based circuit an attractive alternative solution for complete and complicated System-on-Chip designs. This paper presents the ASIC implementation of a unique MASH sigma-delta (Σ - Δ) modulator and an investigation into its hardware architecture. It is demonstrated that the MASH presents an attractive architecture for solutions in System-on-Chip circuits.

2. MODULATOR DESIGN
The block diagram of the implemented
Third-order modulator is shown in Fig. 1.

![Fig.1 digital sections of third-order sigma-delta modulator](image)

The main goal is to develop a topology that can be used for wideband and high-resolution applications, such as audio and telecommunication. Using novel combination of architectural features targets high performance. The techniques used are pipelining, cascade architecture, multibit second stage quantiser, fully interstage scaling, and coefficient optimization. The cascade architecture guarantees robust operation, since the second-order modulators are easily made stable. The pipelining slices the signal path, so that it is possible to achieve high-speed operation. The fully interstage scaling allows us to obtain the highest possible dynamic range, to control the nature of the input signal of the second modulator stage, and also to alter the signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) curve behavior as a function of the input signal amplitude. The multibit quantizer improves the resolution. The used three-bit quantizer produces even poorer resolution than the single-bit quantizer. However, by combining these techniques mentioned above, the effects are illustrated in Fig. 2. The signal/Noise ratio is close to 90Db.

![Fig.2 Simulated signal-to-noise and distortion ratio (SNDR) of third-order sigma-delta](image)

It is advantageous to use as few bits as possible in the quantizer, since the area and the power consumption increase with the number of bits. Those have been implemented in a Digital Power Amplifier. The coefficients are optimized in such a manner that analogue coefficients can be constructed with small integer ratios in order to achieve a compact layout and good matching in the switched-circuit (SC) implementation.

3. MODULATOR IMPLEMENTATION

The Verilog HDL codes are used to implement the MASH3 modulator by using the Silicon Ensemble of the Cadence EDA tools. Many advantages of this implementation, such as low number of multipliers and delays, make this architecture especially attractive for hardware implementation. This is especially true for Digital Power Amplifier implementation. The Digital Power Amplifier is implemented with a 0.6 um CMOS technology utilizing fully differential SC structures. The chip size of the modulator IC is 2.3 x 2.0mm². The targeted modulator resolution is 16 bits with over-sampling.
ratio (OSR) equals to 32, and approximately two bits are reserved for various non-idealities. The target for the sampling rate was specified to be 50 MHz. Following Table 1 shows the coefficient histograms for this modulator, in a typical application. MASH3 modulators are implemented using 3-level quantizers because higher-level quantizers result in smaller quantization noise power.

<table>
<thead>
<tr>
<th>Coeffs</th>
<th>-3</th>
<th>-2</th>
<th>-1</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>MASH3</td>
<td>2</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>24</td>
<td>12</td>
<td>2</td>
</tr>
</tbody>
</table>

*Table 1: Output Coefficient Histograms (%)*

The coefficient histograms in Table 1 demonstrate that, MASH3 architecture is computationally more efficient in noise reduction, it needs 3-bits to encode its output.

4. SUMMARY

Sigma-delta modulations provide high resolution as compared to analogue circuits and could be effectively used to implement various signal-processing algorithms on a System-on-Chip basis (e.g. Digital Power Amplifier). A third-order sigma-delta modulator implementation in Digital Power Amplifier is presented. The operation is obtained by using a novel combination of architectural features, proper circuit structure selections, specific clocking strategies, and efficient circuit optimization algorithms. Measurement results from fabricated CMOS chip prototypes show a good match with simulations.

5. REFERENCES


Acknowledgement

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